REMARKS

This application has been carefully reviewed in light of the Office Action mailed on March 21, 2003. Claims 39, 42 and 45 have been amended. Attached hereto is a marked-up version of the changes made captioned "APPENDIX A." Reconsideration of the above-referenced application in light of the amendments and following remarks is requested.

Claims 39-45 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nakashima in view of Maruyama and Ishikawa. Reconsideration is respectfully requested.

The Office Action contends that "Nakashima discloses all of the limitations except for the memory device connected to a central processing unit." (Office Action, pgs. 2-3). Applicant respectfully submits that Nakashima's layer 4 is not Applicant's claimed single thin layer of material or thin sheet material.

Nakashima teaches mounting a semiconductor chip 3 in the recessed portion of a metal substrate 4 (Col. 7, lines 64-65). Nakashima's semiconductor chip 3 is formed on metal substrate 4. A recess 0 is formed in metal substrate 4 wherein the semiconductor chip 3 is mounted (FIG. 2(a)).

In stark contrast, Applicant's invention is a low profile ball grid array semiconductor package comprising "a base substrate having a top surface and a bottom surface, with an aperture therein which extends from said top surface to said bottom surface," as recited in claims 39 and 45 (emphasis added). Similarly, claim 42 recites "a base substrate having a top surface and a bottom surface, said base substrate having an aperture extending from said top surface to said bottom surface." (emphasis added). Nakashima does not teach or suggest forming an aperture or opening which extends from the top surface to the bottom surface of the substrate as claims 39, 42 and 45 recite. Nakashima merely teaches a recess 0 which is formed within the metal substrate 4.

Moreover, Nakashima does not teach or suggest "a single thin layer of material secured to said base substrate and covering said aperture such that a cavity is formed . . . and a semiconductor element mounted in said cavity," as claim 39 recites, "a single thin layer of material secured to said top surface of said base substrate and covering said aperture to form a downward facing cavity . . . and a semiconductor element mounted in said downward facing cavity," as claim 42 recites, or "a thin sheet material secured to said base substrate and covering said aperture such that a cavity is formed . . . and a semiconductor element mounted in said cavity," as claim 45 recites.

Nakashima teaches that metal substrate 4 is a "support substrate" for mounting semiconductor die 3 (Col. 9, lines 25-26). Nakashima teaches away from forming an aperture that extends from the top surface to the bottom surface of a base substrate and having a single thin layer of material secured to the base substrate to support a semiconductor element. Applicant's base substrate does not support the semiconductor element, a single thin layer or thin shin sheet material supports the semiconductor element.

Still further, Nakashima does not teach or suggest a "single thin layer of material having a thickness of from approximately 0.025 to less than approximately 0.1 mm," as recited in claims 39 and 42. Similarly, claim 45 recites a "thin sheet material having a thickness of from approximately 0.025 to less than approximately 0.1 mm." The Office Action concedes that Nakashima does not teach a "single thin layer of material to be approximately 0.025 to 0.1 mm." (Office Action, page 3).

The Office Action asserts that in Nakashima's Figure 16, the layer of polyimide 13 forms a cavity where a semiconductor die (3) is mounted and is therefore analogous to Applicant's claimed single thin layer of material. Figure 16 clearly illustrates that semiconductor die 3 is supported by multiple layers. Semiconductor die 3 is supported by at least three different layers 1, 2 and 12 and not a "single thin layer of material" as recited in claims 39 and 42 or a "thin sheet of material" as recited in claim 45.

Accordingly, Nakashima does not teach or suggest the limitations of claims 39, 42 and 45. Specifically, Nakashima fails to teach forming a low profile ball grid array package comprising a "base substrate having a top and bottom surface, with an aperture therein which extends from said top surface to said bottom surface . . . [and] a single thin layer of material secured to said base substrate and covering said aperture such that a cavity is formed . . . having a thickness of from approximately 0.025 to less than approximately 0.1 mm," as claim 39 recites, "a base substrate having a top and bottom surface . . . having an aperture extending from said top surface to said bottom surface . . . [and] a single thin layer of material secured to said top surface of said base substrate and covering said aperture to form a downward facing cavity . . . having a thickness of from approximately 0.025 to less than approximately 0.1 mm," as claim 42 recites, or "a base substrate having a top surface and a bottom surface, with an aperture therein which extends from said top surface to said bottom surface . . .[and] a thin sheet material secured to said base substrate and covering said aperture such that a cavity is formed . . . having a thickness of from approximately 0.025 to less than approximately 0.1 mm," as claim 45 recites.

Maruyama is relied upon for teaching a central processing unit and adds nothing to rectify the deficiencies associated with Nakashima. Ishikawa is relied upon for teaching a metal film (20) having a thickness of 0.1 mm with a semiconductor die (40) formed thereon (Office Action, page 3).

For at least the reasons provided above, Nakashima does not teach or suggest a thin sheet material or single thin layer of material which supports a semiconductor element mounted in an aperture that extends from the top surface to the bottom surface of a base substrate. Moreover, Ishikawa teaches away from Applicant's claimed range of thicknesses for the thin sheet material or single thin layer of material.

Ishikawa teaches that the minimum thickness of the metal film should be 0.1 mm or more due to radiation effects and a maximum thickness of 1.0 mm or less due to external connections. Specifically, Ishikawa teaches, "[i]n order to attain sufficient radiation effects, the thickness of the metal film 20 is preferably about 100 μm or more . . .

[and] is preferably 1000 μm or less." (Col. 7, lines 43-46) (emphasis added). Thus, Ishikawa teaches away from using a metal film with a thickness of less than 0.1 mm.

Applicant's invention is directed at providing a low profile ball grid array semiconductor package. Applicant has amended claims 39, 42 and 45 to reflect this important feature of the invention. Specifically, claims 39 and 42 recite a "single thin layer of material having a thickness of from approximately 0.025 to less than approximately 0.1 mm." (emphasis added). Similarly, claim 45 recites a "thin sheet material having a thickness of from approximately 0.025 to less than approximately 0.1 mm." (emphasis added).

For at least these reasons independent claims 39, 42 and 45 should be allowable over the cited combination of references. Claims 40-41 depend from claim 39, and claims 43-44 depend from claim 42. Claims 40-41 and 43-44 contain every limitation of their base claims and should be allowable for at least the same reasons as for allowance of independent claims 39 and 42.

In summary, for all of the reasons set forth above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

By _____

Thomas J. D'Amico
Registration No.: 28,371
DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorney for Applicant

APPENDIX A

39. (Three Times Amended) A processor system comprising:

a central processing unit; and

a memory device connected to said central processing unit, said memory device comprised of a plurality of low profile ball grid array semiconductor packages, said low profile ball grid array semiconductor packages comprised of a base substrate having a top surface and a bottom surface, with an aperture therein which extends from said top surface to said bottom surface,

a series of conductive traces located on one of said top surface and said bottom surface of said base substrate,

a plurality of conductive balls connected to said series of conductive traces,

a single thin layer of material secured to said base substrate and covering said aperture such that a cavity is formed, said single thin layer of material having a thickness of from approximately 0.025 to less than approximately 0.1 mm, and a semiconductor element mounted in said cavity.

42. (twice amended) A processor system comprising:

a central processing unit; and

a memory device connected to said central processing unit, said memory device comprised of a plurality of low profile ball grid array semiconductor packages, said low profile ball grid array semiconductor packages comprised of a base substrate having a top surface and a bottom surface, said base substrate having an aperture extending from said top surface to said bottom surface,

a series of conductive traces located on one of said top surface and said bottom surface of said base substrate,

a plurality of conductive balls connected to said series of conductive traces,

a single thin layer of material secured to said top surface of said base substrate and covering said aperture to form a downward facing cavity, said single thin layer of material having a thickness of from approximately 0.025 to less than approximately 0.1 mm, and a semiconductor element mounted in said downward facing cavity.

45. (Amended) A processor system comprising:

a central processing unit; and

a memory device connected to said central processing unit, said memory device comprised of a plurality of low profile ball grid array semiconductor packages, said low profile ball grid array semiconductor packages comprised of a base substrate having a top surface and a bottom surface, with an aperture therein which extends from said top surface to said bottom surface,

a series of conductive traces located on one of said top surface and said bottom surface of said base substrate,

a plurality of conductive balls connected to said series of conductive traces,

a thin sheet material secured to said base substrate and covering said aperture such that a cavity is formed, said thin sheet material having a thickness of from approximately 0.025 to less than approximately 0.1 mm, and a semiconductor element mounted in said cavity